A BROADBAND LOW NOISE DUAL GATE FET DISTRIBUTED AMPLIFIER

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ABSTRACT

A 2 to 18 GHz monolithic GaAs low noise distributed amplifier has been developed with 10 dB nominal gain. The noise figure is less than 5.7 dB over the 2 to 18 GHz band and less than 4.0 dB from 3 to 13 GHz. The DGFET amplifier provides gain control capability and has low power requirements of 60 mA at 5 volts. This state of the art performance is achieved with a 0.5 μM ion implanted process.

INTRODUCTION

The objective for this project was to design and build a producible, gain controllable, 2 to 18 GHz distributed amplifier, with 10 dB of gain and a noise figure under 6 dB. This paper describes a monolithic DGFET distributed amplifier that meets these objectives. This new amplifier typically provides 1 to 3 dB more single amplifier gain; and 1 to 2 dB better noise figure with approximately half the per amplifier stage power consumption than previously reported FET distributed amplifiers [1, 2, 3, 4]. It provides near equal noise figure and amplifier gain with 58% of the power consumption of a previously reported HEMT distributed amplifier [5]. With 5 volts and 60 mA operating bias, the amplifier has 10 dB nominal gain, input return loss better than 10 dB and output return loss better than 8 dB. The noise figure is less than 5.7 dB from 2 to 18 GHz and under 4.0 dB from 3 to 13 GHz. For still lower power consumption, the amplifier can be operated at 5 volts and 30 mA. With this reduced bias the nominal gain drops to 8 dB and the noise figure degrades by 0.3 dB. Increasing the bias to 7 volts and 90 mA increases the nominal gain to 11 dB while degrading the noise figure by 0.3 dB. This increased bias gives the amplifier medium power capability with a one dB gain compression power output of 18 dBm at 18 GHz This increases to 19 dBm for frequencies below 15 GHz.

The amplifier employs 0.5 μM gate length ion implanted DGFETs and is within the guidelines of the T.I. foundry for optimum producibility. DGFETs were chosen for the increased per stage gain that they provide and for their gain control capability. The principal problem with the use of DGFETs in a distributed amplifier is the experimentally observed tendency to oscillate at frequencies just above the passband. Overcoming this problem required the development of a DGFET equivalent circuit that modeled the oscillation problem and the development of circuit techniques to eliminate the problem.

CIRCUIT DESIGN

The initial design step was to select an appropriate FET process and then determine an adequate equivalent circuit for the DGFET. The underlying assumption was that a DGFET could be considered to be a cascode connection of two intrinsic single gate FETs (FET #1 and FET #2). A further assumption was that the intrinsic equivalent circuits of the two cascoded SGFETs within the DGFET were identical. This assumption was justified by the fact that the FET bias currents would be identical and by the fact that they would be operated at near identical drain to source voltages. An ion implanted 300 μM SGFET with a low-noise/low-current profile was selected as the initial prototype transistor because its equivalent circuit had been determined at 3 volts and 15 mA, and it had demonstrated good (2.5 dB) noise figure performance at 18 GHz.

Preliminary design of the amplifier was based on a DGFET model scaled from the 300 μM SGFET equivalent circuit. The gate line design was based on a constant K low pass filter model with uniform inductance/transmission line sections except for half sections at the ends. The FET gate width and the transmission line lengths were adjusted to obtain a nominal 50 Ohm filter input impedance and a filter cut-off frequency of approximately 20 GHz. This required a DGFET with a gate width of 120 μM. The drain line of uniform M derived filter type with a peaking line between the DGFET drain and the through drain line. The lengths and widths of the drain transmission lines were optimized for minimum amplifier output reflection (S22) and maximum flat gain (S21) up to 20 GHz. the amplifier design required nine 120 μM DGFETs to realize the desired 10 dB gain.

Analysis of the preliminary amplifier design did not show the spurious oscillation tendency predicted by the previous experimental results. Further investigation revealed that the inductance associated

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with the FET #1 source and the FET #2 gate grounds strongly influenced the amplifiers tendency toward instability. This tendency toward instability was indicated by a gain peak that occurred several GHz above the nominally 20 GHz upper passband limit and by an amplifier output reflection coefficient (S22) greater than unity. Common mode inductance between the FET #1 source and the FET #2 gate was particularly detrimental to the amplifier's stability This common mode inductance is caused by the practice of using a common ground via for the FET #1 source and the FET #2 gate. This oscillation tendency is a property of the FET itself because stability analysis of the FET equivalent circuit showed that the ground inductance caused the FET to become potentially unstable at the higher frequencies above 15 GHz.

Even without source inductance, the DGFET is potentially unstable at lower frequencies. This is not a problem in distributed amplifiers because the gate and drain line terminating resistors keep the amplifier from oscillating. At its upper cutoff frequency, the drain-line filter ceases to transmit, effectively isolating the terminating resistor. This presents a reactive impedance to the drain of FET #2. The amplifier oscillation can be eliminated by adding shunt resistance to ground from the drain of the #2 FETs. This reduces amplifier gain so the decision was made to minimize common mode inductance by employing separate ground vias for the FET #1 source and FET #2 gate. The source inductance was further minimized by employing a 2 gate stripe FET with the 2 source stripes directly adjacent to the ground vias The absence of source air bridges over the drain stripe has the additional benefit of reducing feedback capacity.

The accuracy of the DGFET equivalent circuit was improved by measuring a 200 µM DGFET with the same low noise/low current profile material as the 300 µM SGFET. The parameters of the DGFET equivalent circuit were optimized to fit the S-parameters of the measured DGFET. The equivalent circuit parameters of the internal intrinsic FET #1 and FET #2 were forced to be identical during the optimization. The intrinsic FET equivalent circuit values determined from the 200 µM DGFET were similar to those previously determined from the SGFET. The output capacity was somewhat higher, and the magnitude of S11 was significantly higher. The final 120 µM DGFET equivalent circuit used for the amplifier design is shown in Figure 1.

The nodal noise analysis capabilities of Super Compact were used to calculate the noise figure of the amplifier design. This program requires the measured S-parameters and noise parameters of the FET as a data input In the absence of any 120 µM low noise DGFETs to measure, the noise parameters were generated from the FET equivalent circuit values, using Fukui's [6] relationships between FET equivalent circuits and the noise parameters The gate and intrinsic input resistance values of the equivalent circuit were further reduced so that Fukui's equations more nearly duplicated the measured 18 GHz noise figure of the 300 µM SGFET. The S-parameter data required by the nodal noise analysis program was also generated from this revised equivalent circuit Figure 2 shows the

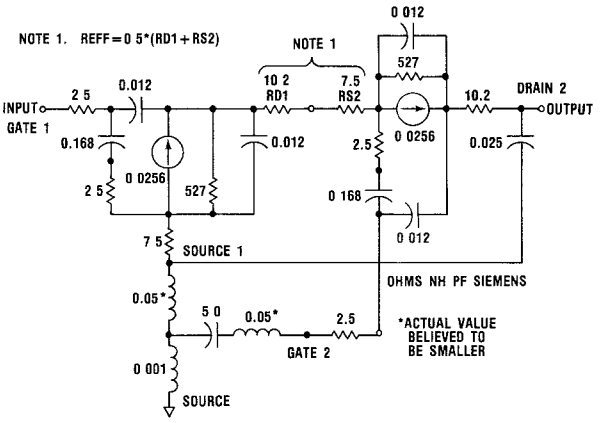

Figure 1. 120 µm DGFET Equivalent Circuit

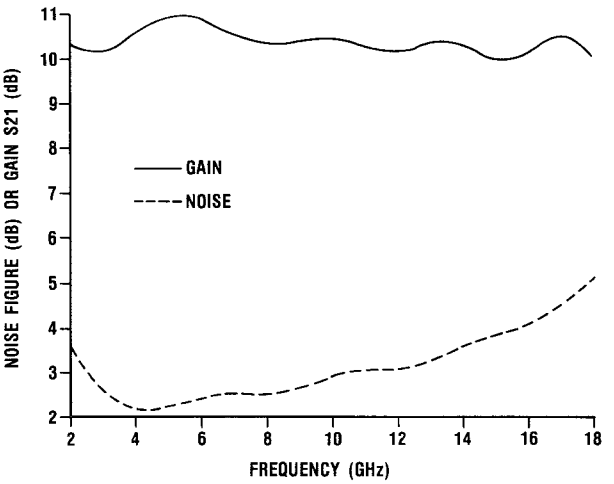

Figure 2. Calculated Gain and Noise Figure

predicted small signal gain and noise figure of the amplifier.

AMPLIFIER CONSTRUCTION

The amplifier was built using the standard T.I. GaAs foundry process which incorporates ground vias, MIM capacitors and air bridges. The amplifier chip is 92 mils wide and 162 mils long, and 4 mils thick. The 9 DGFETs have two 60 µM wide gate stripes each with gate length of 0.5 µM. The FETs employ ion implanted GaAs material with a dual level gate recess and low noise/low current profile. The amplifier has on chip blocking capacitors for the RF input and output. The Gate #1 and Gate #2 terminations have bypass capacitors with additional series resistive isolation to minimize the influence of external components on the amplifier performance. The FET #2 gate bypass capacitors are built on top of the ground vias. An air bridge carries the single drain stripe of the DGFET over the line that interconnects the Gate #2 bypasses. Figure 3 is a photograph of the chip and Figure 4 is a schematic of the amplifier.

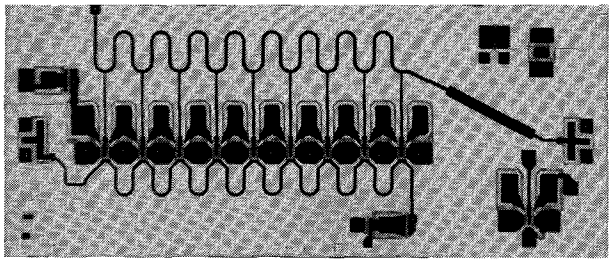

Figure 3. Photograph of Distributed Amplifier

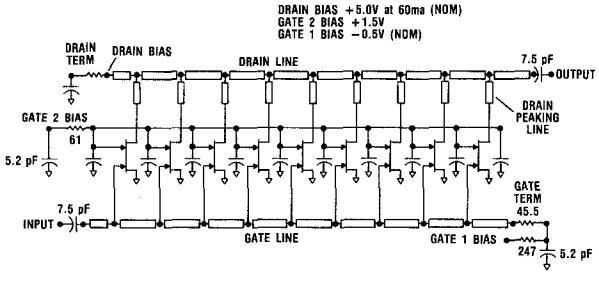

Figure 4. DGFET Distributed Amplifier Schematic

MEASURED RESULTS

Figure 5 shows the measured small signal gain and noise figure of the amplifier operating at the nominal bias of 5.0 volts and 60 mA. The measure performance closely approximates the predicted performance except that the measured noise figure is approximately 0.7 dB higher than the predicted noise

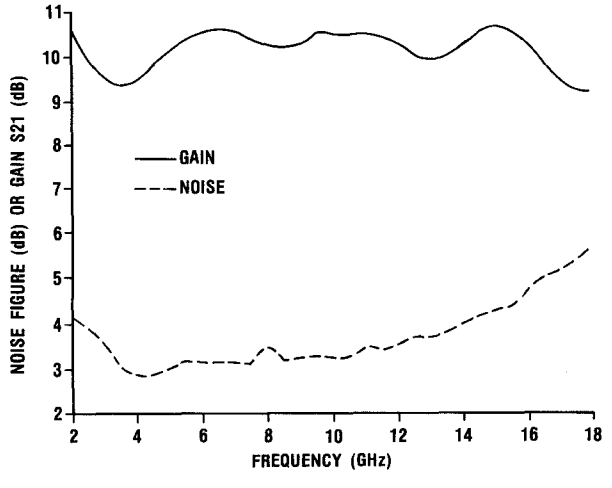

Figure 5. Measured Gain and Noise Figure

figure. Figure 6 shows the RF power output at the 1 dB gain compression point for drain supply currents of 30, 60 and 90 mA. The measured amplifier gain changes approximately 2.0 dB between -50 and +90 degrees C for an average temperature sensitivity of 0.014 dB per degree C. The noise figure is also

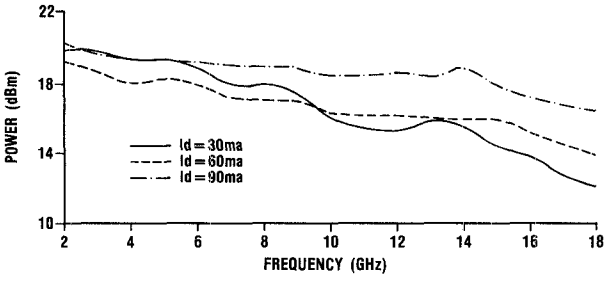

Figure 6. 1 dB Gain Compression Power (VD = 5.0V)

affected by temperature, increasing by 1.3 dB at 90 degrees C and decreasing by 1.1 dB at -50 degrees C, relative to its 25 C 18 GHz value. The amplifier showed no sign of oscillation under any conditions. Six slices were fabricated on this first pass design. Performance of the measured amplifiers is relatively uniform with single frequency noise figure within a 0.4 dB range and midband gain within a 1.5 dB range.

CONCLUSION

A broadband low noise DGFET distributed amplifier with state of the art performance has been designed and built using a standard production process. The agreement between calculated and measured performance is good.

ACKNOWLEDGMENT

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